What is claimed is:

1. A memory device, comprising:

a plurality of addressable memory cells, each memory cell configured to store a first bit and a second bit, each memory cell including:

a first storage circuit configured to store the first bit; and

a second storage circuit configured to store the second bit and coupled to the first storage circuit, and further configured to deactivate the first storage circuit based on the second bit.

2. The memory device of claim 1, further including a first bit line coupled to at least one of the memory cells,

wherein the first storage circuit of the at least one memory cell includes:

an enable node and a first output node, wherein the first storage circuit has either a high or low impedance at the first output node depending upon a logical value of the enable node, the first bit line selectively receiving a logical value of the first output node,

and wherein the second storage circuit of the at least one memory cell includes:

a second output node configured to control the enable node, the first bit line selectively receiving a logical value of the second output node.

3. The memory device of claim 2, further including a second bit line coupled to the at least one memory cell,

wherein the first storage circuit of the at least one memory cell includes:

a third output node, wherein the first storage circuit has either a high or low impedance at the third output node depending upon a logical value of the enable node, the third output node having a logic value opposite the first output node when the first storage circuit has a low impedance at the first and third output nodes, the second bit line selectively receiving a logical value of the third output node,

and wherein the second storage circuit of the at least one memory cell includes:

a fourth output node having a value opposite the second output node, the second bit line selectively receiving a logical value of the fourth output node.

4. The memory device of claim 1, wherein each first storage circuit includes:

a first inverter having an input, an output, and an output enable;

a second inverter having an input, an output, and an output enable, the first and second inverters forming a first latch; and

a first transistor having a source and drain coupled between the output enables of the first and second inverters and a fixed potential, and a gate coupled to the second storage circuit.

5. The memory device of claim 4, wherein each second storage circuit includes a second latch, the gate of the first transistor being coupled to a node of the second latch, a bit line selectively receiving a logical value of the node.

6. An apparatus, comprising:

a plurality of dual-bit memory cells, each memory cell including:

a first storage circuit configured to store a first bit, and

a second storage circuit configured to store a second bit;

a first plurality of word lines each controlling one of the first storage circuits; and

a second plurality of word lines each controlling one of the second storage circuits,

wherein the first storage circuit includes a transistor having a gate, the gate coupled to the second storage circuit so as to receive a value of the second bit.

7. The apparatus of claim 6, wherein the first storage circuit includes a flip flop that stores the first bit and that has a control node, the transistor further coupled between the control node and a fixed potential.

8. The apparatus of claim 6, wherein the second storage circuit includes a flip flop that stores the second bit at a storage node, the gate of the transistor being coupled to the storage node.

9. The apparatus of claim 6, further including a bit line pair each coupled to one of the memory cells, each bit line pair coupled to logic that combines the respective bit line pair into a single logical value.